Data General

Technical Reference

TYPE 4060 ASYNCHRONOUS MULTIPLEXOR

014-000004-04

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The Data General 4060 Asynchronous Multiplexor System enables any Nova-line computer to communicate with and control terminal devices over a variety of communications facilities. The modularity of the 4060 hardware permits simple system expansion, the addition of new features, or the addition of special purpose equipment as the need arises. The 4060 series is supported by software driver package under both RTOS and RDOS.

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SECTION 0

INTRODUCTION

The Data General 4060 Asynchronous Multiplexor System enables any Nova-line computer to communicate with and control terminal devices over a variety of communications facilities. A system is configured from a number of essential and optional subsystems which allow the system characteristics to be adjusted to match the anticipated usage . The modularity of the 4060 hardware permits simple system expansion, the addition of new features, or the addition of special purpose equipment as the need arises. Only asynchronous communication is supported by the multiplexor; the types 4015, 4073, and 4074 communication controllers are available for synchronous or bisynchronous communication. The type 4073 and 4074 can be intermixed with the 4060 series, allowing for one software system responding to a single device code.

The 4060 multiplexor system is unique in that all circuitry required for the multiplexing function is distributed on interface card subsystems each handling four lines. There is no common control circuitry. Each four-line interface card is self-contained; it includes all the circuitry necessary to receive, transmit, and buffer characters for four lines. From 1 to 16 cards serving 4 to 64 lines operate together as a multiplexing system. Such modularity not only minimizes overhead costs for smaller configurations but also localizes most failures to a small group of lines. A single four-line card is a convenient controller for up to four teletypes or higher speed visual display terminals connected locally.

Complete hardware assembly/disassembly and buffering of characters is provided. The software device handler is interrupted only when a new character must be supplied to or accepted from the multiplexor.

The modularity of the 4060 hardware allows, in groups of four lines:

a) Several distinct communications line speeds in a single system (up to 9600 baud).

b) Several transmission codes in a single system (5,6,7, and 8 level with 1, 1½, or 2 stop bits).

c) Easy system expansion from a minimum of four lines to a maximum of 64.

d) Direct (current loop) connection, modem (data set) interface, or modem control for automatic answer.

e) Hardware character assembly/disassembly with full character buffering.

f) Full duplex operation.

g) Four complete line interfaces on each standard Nova-Line subassembly card.

SECTION 1

OPERATION AND SPECIFICATION - GENERAL

In communicating with the terminal or data set, the multiplexor hardware performs all character assembly and disassembly into the serial bit streams required. Start and stop bits are inserted on transmission and stripped out on reception. Character buffering is provided on both reception and transmission so that the program has a full character time to respond without losing input data or reducing transmission rate.

The multiplexor system is flexible in line capacity, transmission code, and line speed. It can accommodate from four to 64 full duplex lines, in multiples of four, at speeds including 9600 baud. The transmission code structure (character size and number of stop bits) and line speeds are selectable by the user so that an installation can be reconfigured with minimal hardware change. Requirements for spare parts are minimal.

A number of four-line receiver/transmitter cards appear as if they were a single I/O device connected to the computer under a single device code. On reception, an I/O instruction reads words containing the line number in the left half and a character in the right. At the completion of transmission of a character, an I/O instruction reads a similar word containing the line number indicating that a character has been transmitted; the program responds by outputting a word containing the appropriate line number and new character. Multiplexing occurs since the I/O instruction to read a line number/character word and control information always effects only one line on one of the several cards. The choice of which of several cards is made automatically by the hardware in priority order, lower line numbers having the higher priority.

At the maximum data rate of the multiplexor system (64 lines each operating at 9600 baud) over 60,000 characters are each received and transmitted every second. Such a data rate allows only 8 microseconds for processing each character; this is inadequate except for trivial operations. Most configurations, however, do not require asynchronous communications at rates exceeding 1200 baud as this rate is currently a standard for the higher speed asynchronous modems and display terminals. At this lower rate, a more

generous amount of processing time is available for each character.

Synchronous communications, using the Data General Type 4015 communications controller which operates through the direct memory access data channel, is more common at speeds of 2400 baud and above for which high performance synchronous modems are available.

Four-line cards physically mounted closer to the processor along the I/O bus have a higher priority in obtaining the processor's attention. Thus, in a system with mixed baud rates, the higher speed lines should be assigned to lower line numbers.

MODELS

Each four-line asynchronous receiver/transmitter card is available in several models. The Type 4060 and 4061 each provide interfacing to four 20 milliampere teletypes. Type 4062 and 4063 provide interfacing to four EIA Type lines either for use with local Teletypes Model 37, Bell System 103-type data sets (modems) or equivalent equipped for manual answer or used on a dedicated line, or other terminal devices with the EIA type interface. The transmitter circuitry examines the Clear to Send signal (Circuit CB) and will not begin transmission of a character unless that control signal is true.

The 4060 and 4062 models come equipped with four individual connectors (9-pin for 800/1200/1230, 50-pin paddle board for 1210/1220/820 series processors) for direct connection of terminal devices or for connection to manual answer modems. The 4061 and 4063 models are provided with a connector arrangement which allows use of the 4050 or 4051 junction panel on 800/1200/1230 and 4083 on 1210/1220/820 series which is described more fully in the cabling section.

		EIA INTERFACE CIRCUITRY	
MODEL		INDIVIDUAL CONNECTORS	DISTRIBUTION BOX
800/ 1200/ 1230	Interface Model	4062	4063
	Conn. or Distribution Box Model No.	4-9 Pin Conn.	4051
820 1210 1220	Interface Model	4062	4063
	Conn. or Distribution Box Model No.	50-Pin Paddle Board	4082

		TTY INTERFACE CIRCUITRY	
MODEL		INDIVIDUAL CONNECTORS	DISTRIBUTION BOX
800/ 1200/ 1230	Interface Model	4060	4061
	Conn. or Distribution Box Model No.	4-9 Pin Conn.	4050
820 1210 1220	Interface Model	4060	4061
	Conn. or Distribution Box Model No.	50-Pin Paddle Board	4082

SECTION 2

RTOS/RDOS SOFTWARE DRIVER

In order to provide a 4060 series communication system which requires the minimal amount of user-program involvement, a device handler was programmed and incorporated in both the Real Time Operating System (RTOS), and the Real Time Disc Operating System (RDOS).

Real Time Operating System is a compatible subset of RDOS. In applications not requiring program overlaying or file naming, it is a flexible, modular interface to user programs in either real-time or off-line environments. Multitasking, timer control, and I/O transfers are handled by simple task and system calls to RTOS. Standard Data General peripherals are supported.

Real Time Disc Operating System is a modular, multitask synchronization and communication system. Tasks may exist in the single mode root program or in an overlay. RDOS operates with any Nova-line computer of 12K or larger memory, disc, real time clock, and Teletype.

RDOS is used in both the development and implementation of programs. It includes all the file capabilities normally available on disc operating systems, allowing the user to edit, assemble, execute, debug, compile, load-and-go, save, and delete files. Files are protected using system defined attributes. File directories are maintained on a fixed head disc and disc pack basis, where each disc pack can be removed from the system. Peripherals are treated as files, providing device independence by symbolic name. Files may be in sequential, random (indexed), and contiguous formats.

The I/O facility includes buffered I/O for ease of programming and unbuffered block transfers for real time applications. Error messages generated in real time can be spooled and output off-line. RDOS supports up to eight fixed head discs or magnetic tape drives, and up to four disc pack units, and all standard Data General peripherals.

Provisions are made for the full use of RTOS and RDOS multitasking capability. Under the initial 4060 series handler release, each line on a system must be dedicated to a separate task.

It is assumed that the reader of this document is sufficiently familiar with either/or RTOS-RDOS file structure and user calls. Refer to RTOS Manual 093-000056 and RDOS Manual 093-000075. Only those calls directly associated with the 4060 series handler will be discussed here.

FILENAME DEFINITION

In RTOS/RDOS each physical input/output device is referred to by some unique filename. In this case, each multiplexed line of the 4060 series corresponds to a filename of the form

QTY: X

where "X" is the multiplexor line number in the range 0 to 63.

OPENING A LINE

Before any reads or writes can occur, a filename or line must be logically connected to a channel number through use of an .OPEN call. The channel number is simply a means by which devices can be referenced in read and write calls without use of a specific file name. This call opens the line for reading or writing. AC0 must contain a byte pointer pointing to the file name. AC1 contains the "characteristic inhibit" mask. For each of the following bits set in the mask, the corresponding characteristic or function is inhibited:

BIT	MNEMONIC*	FUNCTION
10	DCKEY	Echo each input character during a read line.
7	DCPCK	Check for even parity on read line. Generate even parity on write line.
6	DCLAC	Transmit a line feed after each carriage return during a read line or write line.

*All mnemonics refer to user parameters defined on the RTOS/RDOS user parameter list.

EXAMPLE of User OPEN Sequence:

```
        LDA   0,NMPTR   ;GET BYTE POINTER
        LDA   1,MASK    ;INHIBIT MASK
        .SYSTEM
        .OPEN 2         ;2 IS CHANNEL NUMBER
        ERROR RETURN
        NORMAL RETURN
              .
              .
              .
NMPTR:.+1*2
        .TXT*QTY:5*     ;FOR LINE 5
MASK:   DCPCK           ;INHIBIT PARITY CHECKS
```

If the error return were taken, AC2 must be examined for one of the following conditions:

AC2	MNEMONIC	MEANING
0	ERFNO	Illegal channel number.
1	ERFNM	Illegal filename.
12	ERDLE	File does not exit.
21	ERUFT	Attempt to use channel already in use.

CLOSING A LINE

After use, the line must be closed to release the channel assigned to it.

EXAMPLE of Close Sequence:

```
        .SYSTEM
        .CLOSE 2;Channel 2
        ERROR RETURN
        NORMAL RETURN
```

If the error return were taken, AC2 must be examined for one of the following conditions:

AC2	MNEMONIC	MEANING
0	ERFNO	Illegal channel number.
15	ERFOP	Attempt to reference a channel not in use.

READING AND WRITING DATA

GENERAL INFORMATION

In a multitask system such as RDOS, it is possible for the user to do simultaneous reading and writing on one or several 4060 lines through use of the standard input/output calls. The following rules must be noted:

1) No input/output buffering is done within the 4060 driver programs. The read or write call specifies the buffer area to be used. Any data received before a read call for the line is made will be lost.

2) Control is not returned to the calling task until the read or write is completed, that is, all data have been transmitted.

3) Simultaneous reads or writes can be achieved through the creation of a task controlling each line. Simultaneous reading and writing on a given line (full duplex operation) is possible and requires the use of two tasks, one for input and another for output. In full duplex operation, the echo return and line feed insertion features must be inhibited.

READ A LINE

This command causes an ASCII type line to be read. AC0 contains a byte pointer to the starting byte address of the buffer where the data is to be read.

Reading will terminate normally after transmitting either a carriage return, or a form feed to the user. Reading will terminate abnormally after transmission of 132 (decimal) characters without detecting a carriage return or a form feed, upon detection of a parity error, or upon end-of-file (ASCII Sub-Control Z). In all cases, the byte count read will be returned in AC1. If the read is terminated because of a parity error, the character having incorrect parity will be stored (high order bit zero) as the last character read. All characters received will be passed to the user, including NULL's, line feeds, and deletes.

EXAMPLE of Read Sequence:

```
        LDA   0,BPTR
        .SYSTEM
        .RDL   2       ;READ CHANNEL 2
        ERROR RETURN
        NORMAL RETURN
           .
           .
           .
BPTR:   .+1*2
BUF:    .BLK     66.
```

If the error return were taken, AC2 must be examined for one of the following possible conditions:

AC2	MNEMONIC	MEANING
0	ERFNO	Illegal Channel Number.
6	EREOF	End of File.
15	ERFOP	Attempt tc reference a file not opened.
22	ERLLI	Line limit (132 characters) exceeded.
24	ERPAR	Parity Error.
26	ERMEM	Attempt to use illegal memory address.
47	ERSIM	Attempt to read a line already reading.

READ SEQUENTIAL

Sequential mode transmits data exactly as read from the file. AC0 must contain a byte pointer to the starting byte address of the buffer where the data is to be read. There is no end of file code or timeout, and parity bits are not checked.

EXAMPLE of Read Sequential Sequence:

```
LDA  0,BPTR    ;GET BYTE POINTER
LDA  1,COUNT   ;DATA COUNT
.SYSTEM
.RDS  2        ;READ CHANNEL 2
ERROR RETURN
NORMAL RETURN
```

If the error return were taken, AC2 must be examined for one of the following possible conditions:

AC2	MNEMONIC	MEANING
0	ERFNO	Illegal channel number.
15	ERFOP	Attempt to reference a file not opened.
26	ERMEM	Attempt to use illegal memory address.
47	ERSIM	Simultaneous reads on same line.

WRITE A LINE SEQUENCE

AC0 must contain a byte pointer to the starting byte address of the buffer where the data can be found.

Writing will terminate normally upon writing of a null, a carriage return, or a form feed, and abnormally after transmission of 132 (decimal characters) without detection of a carriage return, a null, or a form feed. In all cases, AC1 will contain, upon termination, the number of bytes written from the user area to complete the request.

EXAMPLE of Write a Line Sequence:

```
LDA  0,BPTR    ;GET BYTE POINTER
.SYSTEM
.WRL  2        ;WRITE CHANNEL 2
ERROR RETURN
NORMAL RETURN
```

If an error return were taken, AC2 must be interrogated for one of the following possible conditions:

AC2	MNEMONIC	MEANING
0	ERFNO	Illegal channel number.
15	ERFOP	File not open.
22	ERLLI	Line limit exceeded.
47	ERSIM	Simultaneous writes on same line.

WRITE SEQUENTIAL SEQUENCE

This command writes data exactly as it is found in the user area. AC0 must contain a byte pointer to the starting byte address of the buffer where the data can be found.

EXAMPLE of Write Sequential Sequence:

```
LDA  0,BPTR  ;GET BYTE POINTER
LDA  1,COUNT ;GET BYTE COUNT
.SYSTEM
.WRS 2       ;WRITE CHANNEL 2
ERROR RETURN
NORMAL RETURN
```

If an error return were taken, AC2 must be interrogated for one of the following possible conditions:

AC2	MNEMONIC	MEANING
0	ERFNO	Illegal channel number.
15	ERFOP	File not open.
47	ERSIM	Simultaneous writes on same line.

SECTION 3

PHYSICAL LEVEL PROGRAMMING

A receiver indicator (RI) and a transmit indicator (TI) are associated with each line. The receive indicator is set when a character has been assembled from the serial input stream; it is cleared under program control. The transmit indicator is set whenever the line unit circuitry has accepted a character for transmission and is ready to accept another. I/O reset clears all transmit and receive indicators. Since the transmitter circuitry includes double buffering, the transmit indicator is set almost immediately after accepting the first character following a long idle period. At maximum transmission rate, the transmit indicator is set once per character time; it is cleared under program control.

The four line receiver/transmitter cards contain conventional DONE flags for interface to a Nova-line I/O bus. These are logically ORed together to get a system DONE (QTY DONE). To the programmer, QTY DONE appears set if any input lines have completely assembled characters ready for reading by the processor (some RI=1) or if any output lines have transmitted characters and can accept new characters (some TI=1).

The DIAC instruction, which reads input characters and line control information also clears the receiver indicator of the line just read. Upon issuance of DIAC AC QTY, QTY DONE will be cleared if there are no other lines with data to be read and if all transmit indicators (for all lines) are 0. If there are additional lines to be read or character completions which need be handled, QTY DONE will remain set.

The DOA AC, QTY instruction, which supplies a character for output on a selected line, also clears the transmit indicator for that line. If no new character is to be outputted, the DOB AC, QTY instruction may be used to clear the transmit indicator without sending a new character. While DOA or DOB clears the transmit indicator for a line, they will clear QTY DONE only if there are no other lines on which transmission has completed and if no receivers have assembled characters for the processor to read. The S-pulse is not microcoded as a part of an instruction.

The QTY BUSY flag is set whenever output is occuring on any of the lines. It clears when all characters on all lines awaiting transmission have been sent.

IO INSTRUCTIONS

DIAC AC, QTY reads the following word:

0	1	2–7	8–15
RI	TI	line	Character

RI - Receive indicator -- a character has been assembled and appears in bits 8-15, right justified.

TI - Transmit indicator -- a character previously sent to the transmitter has been accepted for transmission and a new character may be sent.

line - The line number to which the indicators apply.

character - The character just received on the indicated line if RI is set; undefined if RI is not set.

DOA AC, QTY assumes the following word in an accumulator:

0	1	2–7	8–15
		line	character

line - The line number on which the character is to be transmitted and for which the transmit indicator is to be cleared. Bits 0 and 1 are ignored.

character - The character to be transmitted; right justified in the byte if less than 8 bits.

DOB AC, QTY assumes the following word in an accumulator:

0	1	2–7	8–15
		line	

line - The line number (0,1,2 or 3 for a single card system) for which the transmit indicator is to be cleared. Bits 0,1, and 8 through 15 are ignored.

DIA AC, MDM	senses the state of the Ring Indicator signal from 16 lines. AC bit 0 in the logical zero state indicates that line 0 is ringing; AC bit 15 in the logical zero state indicates that line 15 is ringing, etc.
DIB AC, MDM	senses the state of the Data Set Ready signal from 16 lines. A logical one indicates that the data set is ready.
DOA AC, MDM	controls the state of the Data Terminal Ready signal to each of 16 lines. A logical zero in any bit makes the corresponding line ready.

MODEM CONTROL

In order to use a four-line receiver/transmitter card with Bell System 103 Type data sets (modems) or equivalent equipped for automatic answer, additional modem control circuitry is required. This circuitry is not required on lines with manual answer or for dedicated (leased) lines. The control may be provided using the type 4026 interface subassembly with one type 4027 interface for each group of four lines controlled. The 4027 interface provides control of the Data Terminal Ready (Circuit CD) and permits detection of the Ring Indicator (Circuit CE) and Data Set Ready (Circuit CC). Note that the Clear to Send signal and the Carrier Detector signal (Circuit CF) carry identical signals in normal 103 type modem operation; these are examined by the 4062 or 4063 transmitter circuitry. A maximum of four 4027 interfaces can be supplied with each 4026 interface subassembly, which is sufficient to service 16 lines. The required hardware configuration for automatic answer includes: 1) a 4063 multiplexor and a 4027 interface for each group of four or fewer lines and 2) a 4051 junction panel, two 4052A cable assemblies, and a 4026 interface subassembly for each group of 16 lines or less. The purchase order must note that the 4026 is for use as modem control with a 4063 multiplexor system.

In order to use the four-line receiver/transmitter card with Bell System 202 Type data sets (modems) or equivalent equipped for automatic answer on a two wire (half duplex) line or in a multipoint network, control circuitry in addition to that described above is required. A second type 4027 interface is required for each group of four lines so configured. Control is provided for Request to Send and detection facility is provided for Data Carrier and Clear to Send.

SECTION 4

INSTALLATION AND CABLING

CODE SELECTION

A number of transmission codes can be accommodated. Jumpers on the card are used to select line speed, level (number of data bits), and either 1, 1½, or 2 units of stop code. All models are shipped configured for 11 unit, 8 level code at 110 baud; they must be customized by the user for his particular needs. 1½ unit stop code operation is available only with 5 level code (Baudot).

The user can alter the jumper pattern to suit his needs. Select code structure level and units as follows:

Level	Units	Example	Jumpers Installed Level	Jumpers Installed Stop
5	7½	TTY 28		W17,W28
6	8		W13	W17,W29
	9		W13	W17,W18,W29
7	9	IBM 2741	W12	W16,W18,W29
	10		W12	W15,W16,W18,W29
8	10	TTY 37	W12,W13	W15,W16,W19,W29
	11	TTY 33 or 35	W12,W13	W14,W15,W16,W19, W29

Jumpers on the card also determine the four most significant line number address bits. In a system with multiple cards, the card physically mounted closest to the processor card must contain line number group 0 to 3. Line numbers increase as cards are installed further along the I/O bus. Cards are supplied to respond as group 0-3 when ordered individually; when supplied in a system, they are assigned to sequential groups.

Group	Jumpers Installed
0-3	W20,W21,W22,W23
4-7	W20,W21,W22
8-11	W21,W22,W23
12-15	W21,W22
16-19	W20,W21,W23
20-23	W20,W21
24-27	W21,W23
28-31	W21
32-35	W20,W22,W23
36-39	W20,W22
40-43	W22,W23
44-47	W22
48-51	W20,W23
52-55	W20
56-59	W23
60-63	(None)

The line speed is derived from a precision 76.8KC oscillator by the choice of jumpers in a frequency divider chain. Accuracy of the derived frequency is better than .6 of 1%. For frequencies other than those listed above or for more precise control of the frequency, order clock option 4064 and specify the desired baud rate. The crystal frequency will be chosen to be 128 times the baud rate.

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Baud Rate	Jumpers Installed
75	W1,W2,W3,W4,W6,W7,W8
110	W2,W3,W6,W8
134.5	W2,W3,W6
150	W1,W2,W3,W4,W7,W8
300	W1,W2,W3,W4,W8
600	W1,W2,W3,W4
1200	W2,W3,W4
2400	W3,W4
4800	W4
9600	(None)
4064	W1,W2,W3,W4 (Clock Option)

In order to establish a priority order among the several cards in a system, wiring like the INTP wiring on the back panel is required. Connect pin A91 of each four-line card to pin A92 of the next successive four-line card and along the bus.

The installation and cabling scheme is considerably different between the 800/1200 and 1210/1220/820 processor, and therefore will be separated in this document.

800/1200 PROCESSORS

For systems containing only a single card (four lines), individual 9-pin connectors are usually provided on the back of the computer chassis. (See Figure 1). Order Model 4060 or 4062.

A Type 4050 or 4051 junction panel is normally used to interconnect the individual cables from a number of teletypes or data sets (modems) to the multiplexor. Requiring 1-3/4 inches of rack space, the panel contains 16 connectors (4050: 9-pin connectors for Teletype; 4051: 19-pin connectors for data sets (modems)) for attaching the devices and 1 or 2 connectors for connection to the multiplexor and optional automatic answer facility (using 4052 cables). Order Model 4061 or 4063.

In mixed systems (eg; 8 data sets and 4 local Teletypes), the data set (modem) version of the junction panel must be ordered, together with adapter cables which convert the 19-pin connectors to 9 pins for the teletypes. Refer to Example 1 for a sample configuration.

1210/1220/820

For systems requiring up to 16 lines on a 4 slot processor, and up to 32 lines on a 10 slot, the connectors are usually locatable directly on the processor using 1 or 2 4083 16-line connector assemblies. The 4063 EIA and/or 4061 TTY interfaces are used for this configuration. Refer to Example 2 for a sample configuration.

For configurations requiring more connections than allowed according to the above rules or systems where the customer wants a remote connection panel, 50-pin paddle boards are provided. Each of these 50-pin connectors have connections for all of the data leads associated with 1-4060 or 4062 board. Refer to Example 3 for a sample configuration.

MAINTENANCE

A combined diagnostic and reliability test program (tape 095-000073, listing 096-000040) is available for maintenance of a 4060 system. The reliability portion of the test is run to insure satisfactory overall system operation; the diagnostic test is run to localize failures on a board to the failing circuitry. Test plugs are normally used to replace the terminals while tests are run. If the system includes data sets, these often provide a loop-back test mode which performs the same function as the test plug.

EXAMPLE 1:

For 1200/800 type processors. See Figure 2 for diagram of this example.

A typical Nova 1200 computer based communication system with 12 lines attached to 103 Bell System data sets (modems) with automatic answer and four local teletypes.

REQUIRED:

1 - 1200/800/1230 Type Nova Line computer plus core memory.

1 - 4061 four-line asynchronous receiver/transmitter equipped for 20 ma. TTY interface.

3 - 4063 four-line asynchronous receiver/transmitter equipped for EIA type interface.

1 - 4026 Interface subassembly

3 - 4027 EIA type interfaces

1 - 4051 Data set junction panel

2 - 4052A Cable for connecting one 4026 and the 4063-4061 combination to the 4051

4 - 1020A Connector adapters

OPTIONAL:

12 - 1018A Interconnect cable for 4051 to 103 data set (modem)

4 - 4010A or 4010E 33 ASR Teletypes

4 - 1019A Extension cables for use with 4010.

FIGURE 1

TYPICAL 4 LINE CONFIGURATION

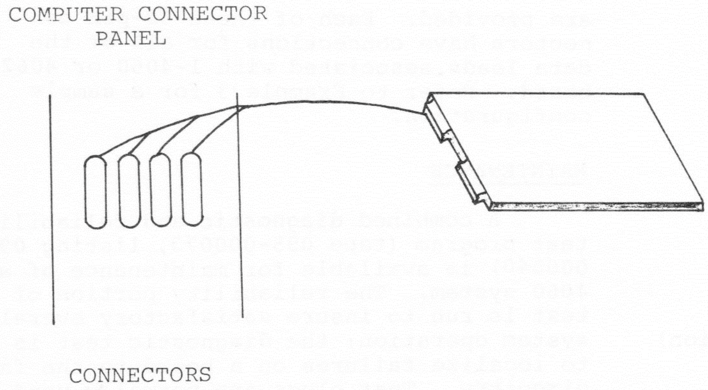
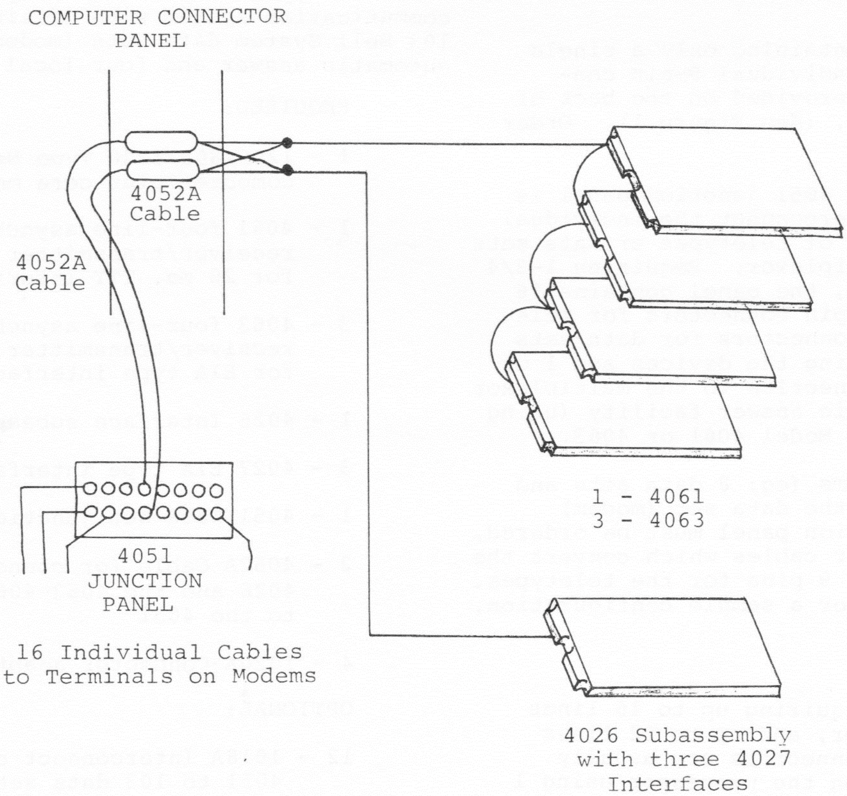


FIGURE 2

TYPICAL 16 LINE 4060 SYSTEM

(As given in configuration example #1)



EXAMPLE 2

For 1210,1220,820 processors using 4083 connector panel. (See Figure 4)

A typical computer based communication system with 12 lines attached to 103 Bell System data sets (modems) with automatic answer and four local Teletypes.

REQUIRED:

1 - Any Nova-line computer plus core memory.
1 - 4061 four-line asynchornous receiver/transmitter equipped for 20 ma. TTY interface.
3 - 4063 four-line asynchronous receiver/transmitter equipped for EIA type interface.
1 - 4026 Interface subassembly
3 - 4027 EIA type interfaces
1 - 4083 Connector panel ordered as:

#4083 - 16-LINE CONNECTOR

Line #	Description
0	1st 4061 - TTY Interface
1	1st 4061 - TTY Interface
2	1st 4061 - TTY Interface
3	1st 4061 - TTY Interface
4	1st 4063/4026 EIA w/Modem Control Interface
5	1st 4063/4026 EIA w/Modem Control Interface
6	1st 4063/4026 EIA w/Modem Control Interface
7	1st 4063/4026 EIA w/Modem Control Interface
8	2nd 4063/4026 EIA w/Modem Control Interface
9	2nd 4063/4026 EIA w/Modem Control Interface
10	2nd 4063/4026 EIA w/Modem Control Interface
11	2nd 4063/4026 EIA w/Modem Control Interface
12	3rd 4063/4026 EIA w/Modem Control Interface
13	3rd 4063/4026 EIA w/Modem Control Interface
14	3rd 4063/4026 EIA w/Modem Control Interface
15	3rd 4063/4026 EIA w/Modem Control Interface

OPTIONAL:

12 - 1049-G Interconnecting cables from 4083 to Modem

4 - 1019-G Extension cables for use with 4010

4 - 4010A or 4010E 33 ASR Teletypes

EXAMPLE 3

For 1210,1220,820 processors using 50-pin paddle board connectors.

CONFIGURATION EXAMPLE

A typical computer based communication system with 12 lines attached to 103 Bell System data sets (modems) with automatic answer and four local Teletypes.* No external cable is available from Data General to interface an Auto Answer Modem to 50-pin paddle boards. No internal cross wiring is done between the 4063's and the 4026/27 Modem Control. See Figure 3 for graphic presentation of this example.

REQUIRED:

1 - Any Nova-line computer plus core memory
1 - 4061 four-line asynchronous receiver/transmitter equipped for 20 ma. TTY interface.
3 - 4063 four-line asynchronous receiver/transmitter equipped for EIA type interface
1 - 4026 Interface subassembly
3 - 4027 EIA type interfaces

OPTIONAL:

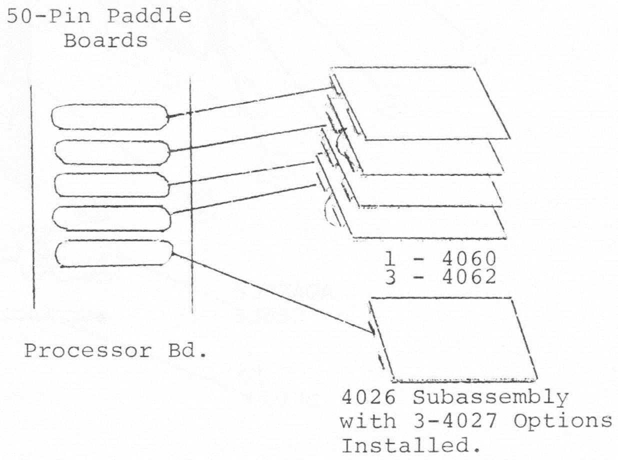
4 - 1019B Extension cables for use with 4010

4 - 4010A or 4010E 33ASR Teletypes

* (See Figure 4)

FIGURE 3

Typical 16 line system for 1210,1220, 820 system processors -- As given in Example 3.



ITEM	DESCRIPTION
1	P4 BACKPANEL SLOT 9
2	P5 PAPER TAPE READER OPTION 4011B
3	P6 EIA OPTION 4023
4	P7 PAPER TAPE PUNCH OPTION 4012A
5	4083 CONNECTOR ASSEMBLY OPTION
6	13 PIN(S) CONNECTOR
7	P2 TELETYPEWRITER INTERFACE CONNECTOR
8	50 PIN PADDLE BOARD

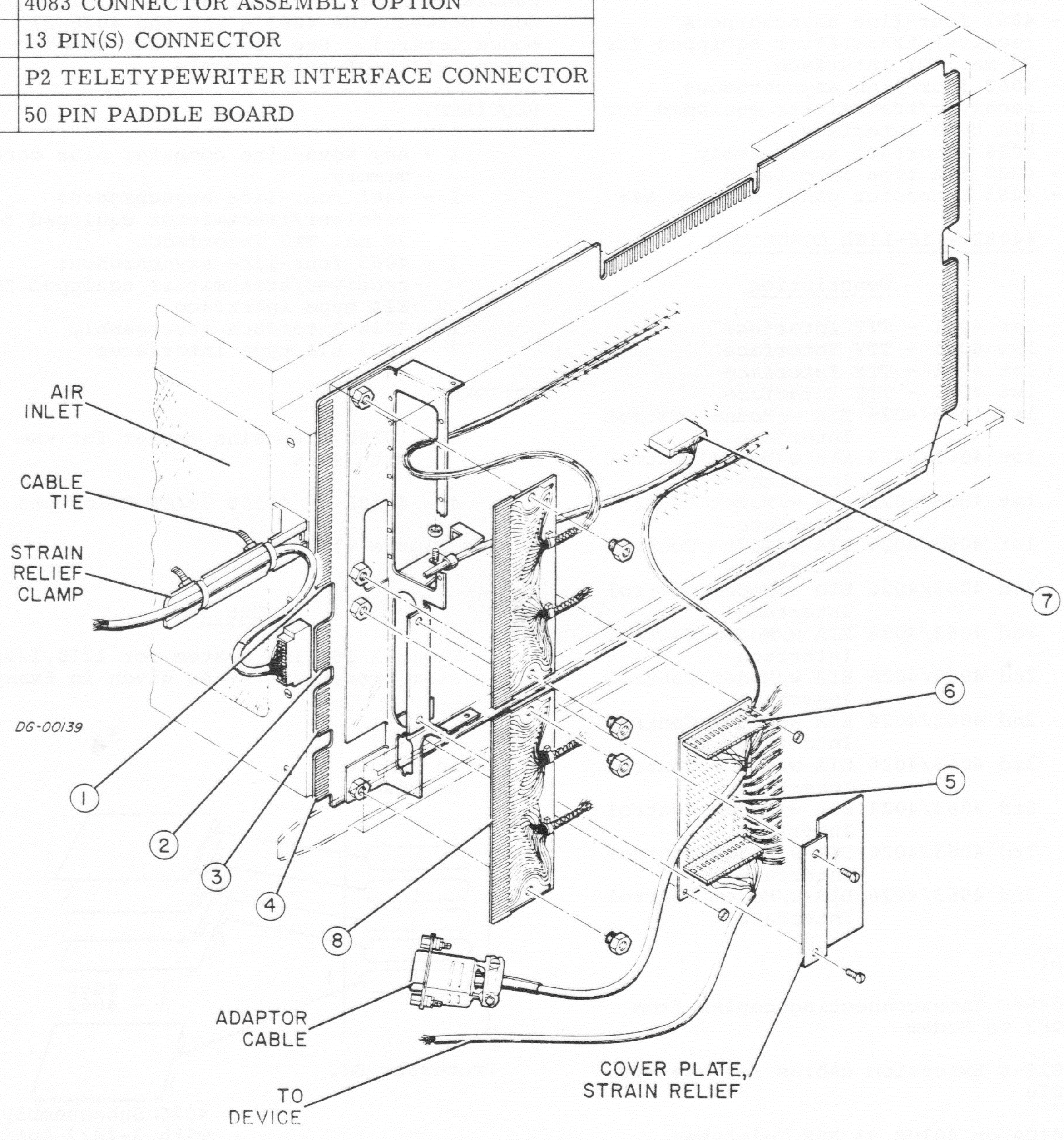


Figure 4 Sketch of the Nova 1220 & 820 Cabling Scheme. The 1210 Cabling is similiar, except it has half the capacity for connectors. Note that the 4083 Connector Panel is physically attached to the Processor.

SECTION 5

THEORY OF OPERATION

Each four-line card contains five major sections including:

a) Interface to computer I/O system.

b) Interface circuitry (either 20 ma. loop or EIA) to match the TTL logic circuitry to the communications lines.

c) Clock oscillator and divider chain.

d) Four buffered serial to parallel receivers.

e) Four buffered parallel to serial transmitters.

The computer I/O interface circuitry performs few functions beyond decoding I/O instructions so that one of the receivers or transmitters on the card can respond appropriately. It provides priority chain logic which functions much like INTP IN/OUT so that only one card responds to I/O instructions at any time. The clock circuitry is a straightforward oscillator and divider which provides a clock signal at eight times the baud rate.

The transmitter circuitry comprises a parallel buffer register and a shift register. When the buffer empties, a program interrupt is generated and a character is requested from the processor. When a character is outputted, it is first loaded into and held in the parallel register. At any integral number of bit times after the last stop bit of the previous character has begun, the serial register is available for loading from the parallel holding register. When loaded, a starting space is put on the line and the shift register is enabled to shift every bit time thereafter.

The end of a character is detected by examining the code pattern which was shifted into the transmitter as the character bits were outputted.

Operation of the receiver is the reverse of the transmitter. A serial bit stream is assembled in a shift register and then, fully assembled, it is loaded into a parallel holding register which, in turn, interfaces to the programmed I/O facility. The only complex part of the operation centers around synchronization of the receiver to the incoming bit stream. The line is examined for a space which, when detected, enables a divide-by-eight circuit. Should the line immediately return to the marking state, the space is ignored as extraneous noise. Should the line remain spacing for 1/2 bit time, the divide-by-eight circuitry produces a clock signal in the center of each bit interval.

TABLE 1

Wiring to connect four or fewer TTY lines to 9-pin Cannon connectors on 1200/800/1230 type processors:

FROM	SIGNAL NAME	BACK PANEL
1	+5	3,4,97,98
2	Reader Run/GND	1,2,99,100
3	Received Data	A87,A88,A89,A90*
4	Ground	1,2,99,100
5	(Not Used)	
6	Ground	1,2,99,100
7	Transmitted Data	A85,A86,A83,A84*
8	(Not Used)	
9	Ground	1,2,99,100

*Sockets 0-3 respectively.

TABLE 2

Wiring to connect four or fewer EIA dedicated lines to 19-pin Cannon connectors on 1200/800/1230 type processors.

FROM	SIGNAL NAME	BACK PANEL
1	Ground	1,2,99,100
2	TX Data	A85,A86,A83,A84*
3	RC Data	A87,A88,A89,A90*
5	Clr. To Snd.	A75,A77,A76,A78*

*Sockets 0-3 respectively.

TABLE 3

Wiring to connect 4061 TTY lines to 13-pin connector on 4083.

FROM	SIGNAL NAME	BACK PANEL
1	Data Out	A85,A86,A83,A84*
2	Ground	99
4	RDR/RN (6 round)	1,2,99,100
8	+5	3,4,97,98
9	Ground	99
11	Rec. Data	A87,A88,A89,A90*
12	Ground	99

*Sockets 0-3 respectively.

TABLE 4

Wiring to connect 4063 EIA to 13-pin connectors on 4083. Table is shown with 402 4026/4027 modem control option. If option is not included, pin 5 of each 13-pin connector is strapped to processor +5.

FROM 4083	NAME OF SIGNAL	TO BACK PANEL
	GND	A99
C1-2	Transmitted Data 0	A85 1st 4060 Slot
C2-2	Transmitted Data 1	A86 1st 4060 Slot
C3-2	Transmitted Data 2	A83 1st 4060 Slot
C4-2	Transmitted Data 3	A84 1st 4060 Slot
C5-2	Transmitted Data 4	A85 2nd 4060 Slot
C6-2	Transmitted Data 5	A86 2nd 4060 Slot
C7-2	Transmitted Data 6	A83 2nd 4060 Slot
C8-2	Transmitted Data 7	A84 2nd 4060 Slot
C9-2	Transmitted Data 8	A85 3rd 4060 Slot
C10-2	Transmitted Data 9	A86 3rd 4060 Slot
C11-2	Transmitted Data 10	A83 3rd 4060 Slot
C12-2	Transmitted Data 11	A84 3rd 4060 Slot
C13-2	Transmitted Data 12	A85 4th 4060 Slot
C14-2	Transmitted Data 13	A86 4th 4060 Slot
C15-2	Transmitted Data 14	A83 4th 4060 Slot
C16-2	Transmitted Data 15	A84 4th 4060 Slot
C1-11	Received Data 0	A87 1st 4060 Slot
C2-11	Received Data 1	A88 1st 4060 Slot
C3-11	Received Data 2	A89 1st 4060 Slot
C4-11	Received Data 3	A90 1st 4060 Slot
C5-11	Received Data 4	A87 2nd 4060 Slot
C6-11	Received Data 5	A88 2nd 4060 Slot
C7-11	Received Data 6	A89 2nd 4060 Slot
C8-11	Received Data 7	A90 2nd 4060 Slot
C9-11	Received Data 8	A87 3rd 4060 Slot
C10-11	Received Data 9	A88 3rd 4060 Slot
C11-11	Received Data 10	A89 3rd 4060 Slot
C12-11	Received Data 11	A90 3rd 4060 Slot
C13-11	Received Data 12	A87 4th 4060 Slot
C14-11	Received Data 13	A88 4th 4060 Slot
C15-11	Received Data 14	A89 4th 4060 Slot
C16-11	Received Data 15	A90 4th 4060 Slot
C1-3	Ring Indicator 0	B69 4026 Slot
C2-3	Ring Indicator 1	B67 4026 Slot
C3-3	Ring Indicator 2	B53 4026 Slot
C4-3	Ring Indicator 3	B52 4026 Slot
C5-3	Ring Indicator 4	B40 4026 Slot
C6-3	Ring Indicator 5	B38 4026 Slot
C7-3	Ring Indicator 6	B25 4026 Slot
C8-3	Ring Indicator 7	B23 4026 Slot
C9-3	Ring Indicator 8	A89 4026 Slot
C10-3	Ring Indicator 9	A88 4026 Slot
C11-3	Ring Indicator 10	A87 4026 Slot
C12-3	Ring Indicator 11	A86 4026 Slot
C13-3	Ring Indicator 12	A75 4026 Slot
C14-3	Ring Indicator 13	A65 4026 Slot
C15-3	Ring Indicator 14	A63 4026 Slot
C16-3	Ring Indicator 15	A61 4026 Slot

FROM 4083	NAME OF SIGNAL	TO BACK PANEL
	GND	
C1-6	Clear to Send 0	A75 1st 4060 Slot
C2-6	Clear to Send 1	A77 1st 4060 Slot
C3-6	Clear to Send 2	A76 1st 4060 Slot
C4-6	Clear to Send 3	A78 1st 4060 Slot
C5-6	Clear to Send 4	A75 2nd 4060 Slot
C6-6	Clear to Send 5	A77 2nd 4060 Slot
C7-6	Clear to Send 6	A76 2nd 4060 Slot
C8-6	Clear to Send 7	A78 2nd 4060 Slot
C9-6	Clear to Send 8	A75 3rd 4060 Slot
C10-6	Clear to Send 9	A77 3rd 4060 Slot
C11-6	Clear to Send 10	A76 3rd 4060 Slot
C12-6	Clear to Send 11	A78 3rd 4060 Slot
C13-6	Clear to Send 12	A75 4th 4060 Slot
C14-6	Clear to Send 13	A77 4th 4060 Slot
C15-6	Clear to Send 14	A76 4th 4060 Slot
C16-6	Clear to Send 15	A78 4th 4060 Slot
C1-5	Data Terminal Ready 0	B54 4026 Slot
C2-5	Data Terminal Ready 1	B51 4026 Slot
C3-5	Data Terminal Ready 2	B49 4026 Slot
C4-5	Data Terminal Ready 3	B48 4026 Slot
C5-5	Data Terminal Ready 4	B19 4026 Slot
C6-5	Data Terminal Ready 5	B15 4026 Slot
C7-5	Data Terminal Ready 6	B13 4026 Slot
C8-5	Data Terminal Ready 7	B11 4026 Slot
C9-5	Data Terminal Ready 8	B6 4026 Slot
C10-5	Data Terminal Ready 9	A92 4026 Slot
C11-5	Data Terminal Ready 10	A91 4026 Slot
C12-5	Data Terminal Ready 11	A90 4026 Slot
C13-5	Data Terminal Ready 12	A59 4026 Slot
C14-5	Data Terminal Ready 13	A57 4026 Slot
C15-5	Data Terminal Ready 14	A49 4026 Slot
C16-5	Data Terminal REady 15	A47 4026 Slot
C1-7	Data Set Ready 0	B27 4026 Slot
C2-7	Data Set Ready 1	B34 4026 Slot
C3-7	Data Set Ready 2	B31 4026 Slot
C4-7	Data Set Ready 3	B36 4026 Slot
C5-7	Data Set Ready 4	A85 4026 Slot
C6-7	Data Set Ready 5	A84 4026 Slot
C7-7	Data Set Ready 6	A81 4026 Slot
C8-7	Data Set Ready 7	A83 4026 Slot
C9-7	Data Set Ready 8	A78 4026 Slot
C10-7	Data Set Ready 9	A79 4026 Slot
C11-7	Data Set Ready 10	A76 4026 Slot
C12-7	Data Set Ready 11	A77 4026 Slot
C13-7	Data Set Ready 12	A73 4026 Slot
C14-7	Data Set Ready 13	A71 4026 Slot
C15-7	Data Set Ready 14	A67 4026 Slot
C16-7	Data Set Ready 15	A69 4026 Slot
C1,16,7	GND	
	GND	
C1-16,Pin 12&8	+5V	

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TABLE 5

Wiring to connect TTY interface to 4050 junction box with 4052A cables, on 1200/800/1230 type processors.

FROM	Boards	NAME OF SIGNAL	TO BACK PANEL
1		GND	A99
2	4 Boards (2–17); 3 Boards (2–13); 2 Boards (2–9)	Recvd Data 0	A87 Slot N
3		Recvd Data 1	A88 Slot N
4		Recvd Data 2	A89 Slot N
5		Recvd Data 3	A90 Slot N
6		Recvd Data 4	A87 Slot N+1
7		Recvd Data 5	A88 Slot N+1
8		Recvd Data 6	A89 Slot N+1
9		Recvd Data 7	A90 Slot N+1
10		Recvd Data 8	A87 Slot N+2
11		Recvd Data 9	A88 Slot N+2
12		Recvd Data 10	A89 Slot N+2
13		Recvd Data 11	A90 Slot N+2
14		Recvd Data 12	A87 Slot N+3
15		Recvd Data 13	A88 Slot N+3
16		Recvd Data 14	A89 Slot N+3
17		Recvd Data 15	A90 Slot N+3
18	4 Boards (18–33); 3 Boards (18–29); 2 Boards (18–25); 1 Bd (18–21)	Trans.Data 0	A85 Slot N
19		Trans.Data 1	A86 Slot N
20		Trans.Data 2	A83 Slot N
21		Trans.Data 3	A84 Slot N
22		Trans.Data 4	A85 Slot N+1
23		Trans.Data 5	A86 Slot N+1
24		Trans.Data 6	A83 Slot N+1
25		Trans.Data 7	A84 Slot N+1
26		Trans.Data 8	A85 Slot N+2
27		Trans.Data 9	A86 Slot N+2
28		Trans.Data 10	A83 Slot N+2
29		Trans.Data 11	A84 Slot N+2
30		Trans.Data 12	A85 Slot N+3
31		Trans.Data 13	A86 Slot N+3
32		Trans.Data 14	A83 Slot N+3
33		Trans.Data 15	A84 Slot N+3
50		GND	99
51		GND	100
52		+5V	97

TABLE 6

Wiring to connect 4063's and 4026/27 to 4051 junction box for 1200/800/1230 type processors.

For connector 16 of 4051:

FROM	Boards	NAME OF SIGNAL	TO BACK PANEL
1		GND	A99
2	4 Boards (2–17); 3 Boards (2–13); 2 Boards (2–9); 1 Bd (2–5)	Recvd Data 0	A87 1st 4060 Slt.
3		Recvd Data 1	A88 1st 4060 Slt.
4		Recvd Data 2	A89 1st 4060 Slt.
5		Recvd Data 3	A90 1st 4060 Slt.
6		Recvd Data 4	A87 2nd 4060 Slt.
7		Recvd Data 5	A88 2nd 4060 Slt.
8		Recvd Data 6	A89 2nd 4060 Slt.
9		Recvd Data 7	A90 2nd 4060 Slt.
10		Recvd Data 8	A87 3rd 4060 Slt.
11		Recvd Data 9	A88 3rd 4060 Slt.
12		Recvd Data 10	A89 3rd 4060 Slt.
13		Recvd Data 11	A90 3rd 4060 Slt.
14		Recvd Data 12	A87 4th 4060 Slt.
15		Recvd Data 13	A88 4th 4060 Slt.
16		Recvd Data 14	A89 4th 4060 Slt.
17		Recvd Data 15	A90 4th 4060 Slt.
18	4 Boards (18–33); 3 Boards (18–29); 2 Boards (18–25); 1 Bd (18–21)	Trans.Data 0	A85 1st 4060 Slt.
19		Trans.Data 1	A86 1st 4060 Slt.
20		Trans.Data 2	A83 1st 4060 Slt.
21		Trans.Data 3	A84 1st 4060 Slt.
22		Trans.Data 4	A85 2nd 4060 Slt.
23		Trans.Data 5	A86 2nd 4060 Slt.
24		Trans.Data 6	A83 2nd 4060 Slt.
25		Trans.Data 7	A84 2nd 4060 Slt.
26		Trans.Data 8	A85 3rd 4060 Slt.
27		Trans.Data 9	A86 3rd 4060 Slt.
28		Trans.Data 10	A83 3rd 4060 Slt.
29		Trans.Data 11	A84 3rd 4060 Slt.
30		Trans.Data 12	A85 4th 4060 Slt.
31		Trans.Data 13	A86 4th 4060 Slt.
32		Trans.Data 14	A83 4th 4060 Slt.
33		Trans.Data 15	A84 4th 4060 Slt.
34		Ring Ind. 0	B69 4026 Slt.
35		Ring Ind. 1	B67 4026 Slt.
36		Ring Ind. 2	B53 4026 Slt.
37		Ring Ind. 3	B52 4026 Slt.
38		Ring Ind. 4	B40 4026 Slt.
39		Ring Ind. 5	B38 4026 Slt.
40		Ring Ind. 6	B25 4026 Slt.
41		Ring Ind. 7	B23 4026 Slt.
42		Ring Ind. 8	A89 4026 Slt.
43		Ring Ind. 9	A88 4026 Slt.
44		Ring Ind. 10	A87 4026 Slt.
45		Ring Ind. 11	A86 4026 Slt.
46		Ring Ind. 12	A75 4026 Slt.
47		Ring Ind. 13	A65 4026 Slt.
48		Ring Ind. 14	A63 4026 Slt.
49		Ring Ind. 15	A61 4026 Slt.
50		GND	
51		GND	
52		+5V	

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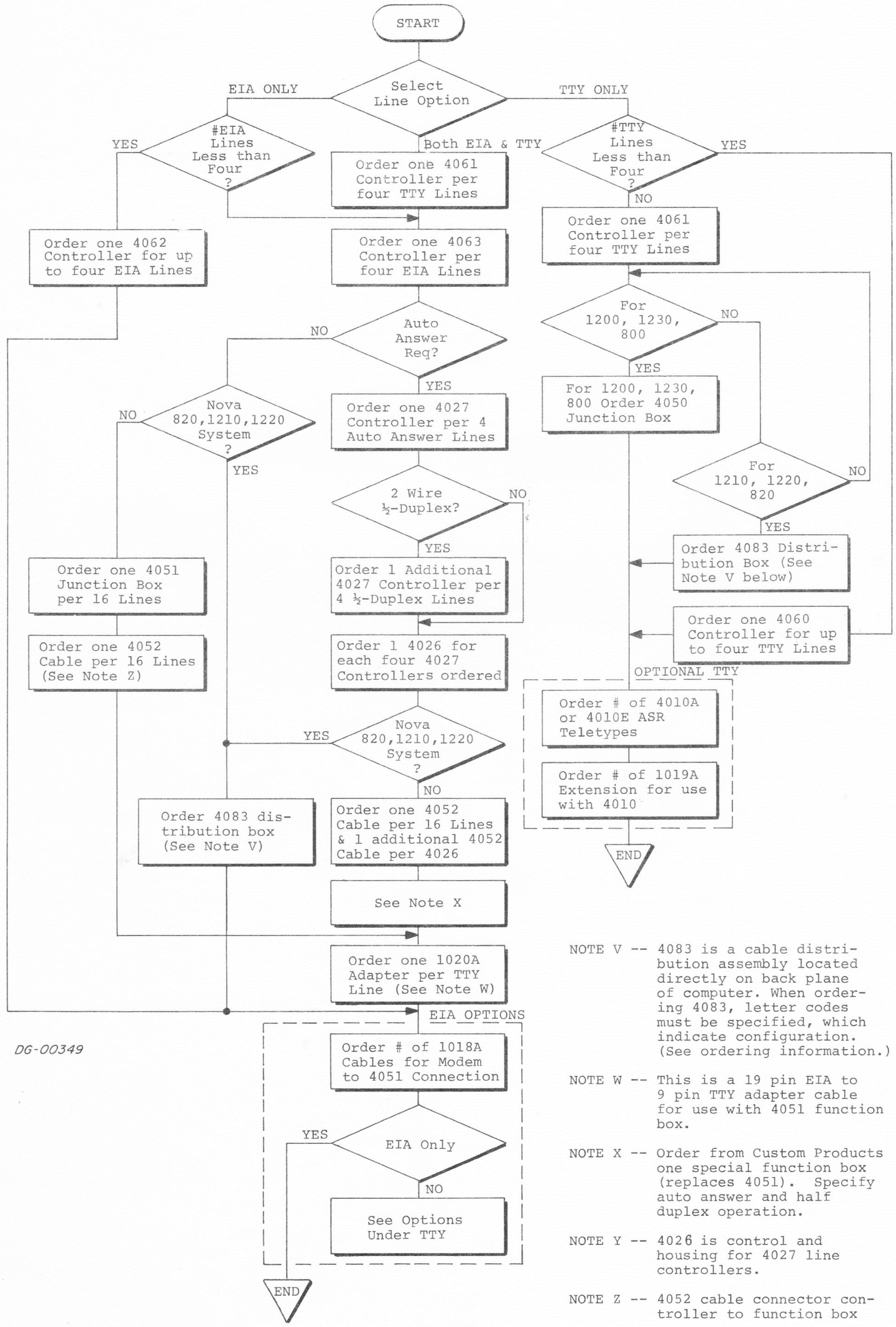
For connector 17 of 4051:

1Bd / 2 Boards / 3 Boards / 4 Boards

FROM	NAME OF SIGNAL	TO BACK PANEL
1	GND	
2	Clr. to Send 0	A75 1st 4060 slt.
3	Clr. to Send 1	A77 1st 4060 slt.
4	Clr. to Send 2	A76 1st 4060 slt.
5	Clr. to Send 3	A78 1st 4060 slt.
6	Clr. to Send 4	A75 2nd 4060 slt.
7	Clr. to Send 5	A77 2nd 4060 slt.
8	Clr. to Send 6	A76 2nd 4060 slt.
9	Clr. to Send 7	A78 2nd 4060 slt.
10	Clr. to Send 8	A75 3rd 4060 slt.
11	Clr. to Send 9	A77 3rd 4060 slt.
12	Clr. to Send 10	A76 3rd 4060 slt.
13	Clr. to Send 11	A78 3rd 4060 slt.
14	Clr. to Send 12	A75 4th 4060 slt.
15	Clr. to Send 13	A77 4th 4060 slt.
16	Clr. to Send 14	A76 4th 4060 slt.
17	Clr. to Send 15	A78 4th 4060 slt.
18	Data Term. Rdy. 0	B54 4026 slot
19	Data Term. Rdy. 1	B51 4026 slot
20	Data Term. Rdy. 2	B49 4026 slot
21	Data Term. Rdy. 3	B48 4026 slot
23	Data Term. Rdy. 4	B19 4026 slot
24	Data Term. Rdy. 5	B15 4026 slot
25	Data Term. Rdy. 6	B13 4026 slot
26	Data Term. Rdy. 7	B11 4026 slot
27	Data Term. Rdy. 8	B6 4026 slot
28	Data Term. Rdy. 9	A92 4026 slot
29	Data Term. Rdy. 10	A91 4026 slot
30	Data Term. Rdy. 11	A90 4026 slot
31	Data Term. Rdy. 12	A59 4026 slot
32	Data Term. Rdy. 13	A57 4026 slot
33	Data Term. Rdy. 14	A49 4026 slot
34	Data Term. Rdy. 15	A47 4026 slot
35	Data Set Rdy. 0	B27 4026 slot
36	Data Set Rdy. 1	B34 4026 slot
37	Data Set Rdy. 2	B31 4026 slot
38	Data Set Rdy. 3	B36 4026 slot
39	Data Set Rdy. 4	A85 4026 slot
40	Data Set Rdy. 5	A84 4026 slot
41	Data Set Rdy. 6	A81 4026 slot
42	Data Set Rdy. 7	A83 4026 slot
43	Data Set Rdy. 8	A78 4026 slot
44	Data Set Rdy. 9	A79 4026 slot
45	Data Set Rdy. 10	A76 4026 slot
46	Data Set Rdy. 11	A77 4026 slot
47	Data Set Rdy. 12	A73 4026 slot
48	Data Set Rdy. 13	A71 4026 slot
49	Data Set Rdy. 14	A67 4026 slot
50	Data Set Rdy 15	A69 4026 slot
51	GND	
52	GND	
	+5V	

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4060 SYSTEM CONFIGURATOR



DG-00349

NOTE V -- 4083 is a cable distribution assembly located directly on back plane of computer. When ordering 4083, letter codes must be specified, which indicate configuration. (See ordering information.)

NOTE W -- This is a 19 pin EIA to 9 pin TTY adapter cable for use with 4051 function box.

NOTE X -- Order from Custom Products one special function box (replaces 4051). Specify auto answer and half duplex operation.

NOTE Y -- 4026 is control and housing for 4027 line controllers.

NOTE Z -- 4052 cable connector controller to function box

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- ☐ Government

2. Hardware

	Qty. Installed	Qty. On Order
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C/350, C/330, C/300		
S/250, S/230, S/200		
S/130		
AP/130		
CS Series		
N3/D		
Other NOVA		
microNOVA		
Other (Specify) ______		
______		
______		

3. Software

- ☐ AOS
- ☐ DOS
- ☐ SOS
- ☐ RDOS
- ☐ RTOS
- ☐ Other

Specify ______________

4. Languages

- ☐ Algol
- ☐ DG/L
- ☐ Cobol
- ☐ ECLIPSE Cobol
- ☐ Business BASIC
- ☐ BASIC
- ☐ Assembler
- ☐ Interactive
- ☐ Fortran
- ☐ RPG II
- ☐ PL/1
- ☐ Other

Specify ______________

5. Mode of Operation

- ☐ Batch (Central)
- ☐ Batch (Via RJE)
- ☐ On-Line Interactive

6. Communications

- ☐ RSTCP
- ☐ HASP
- ☐ RJE80
- ☐ SAM
- ☐ CAM
- ☐ 4025
- ☐ Other

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○ ______________

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- ☐ Other

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